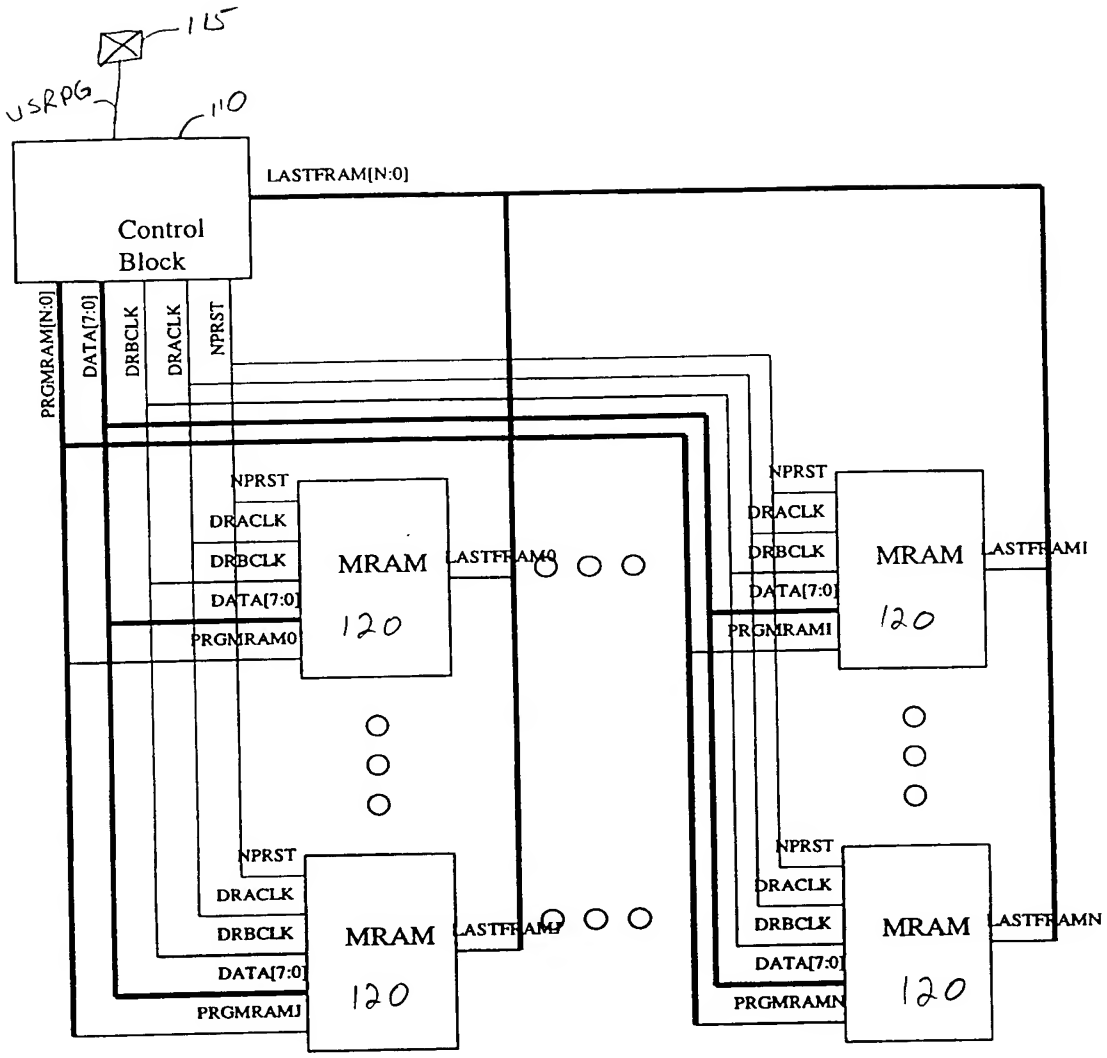

Figure 1: Chip level block diagram of MRAM preload.

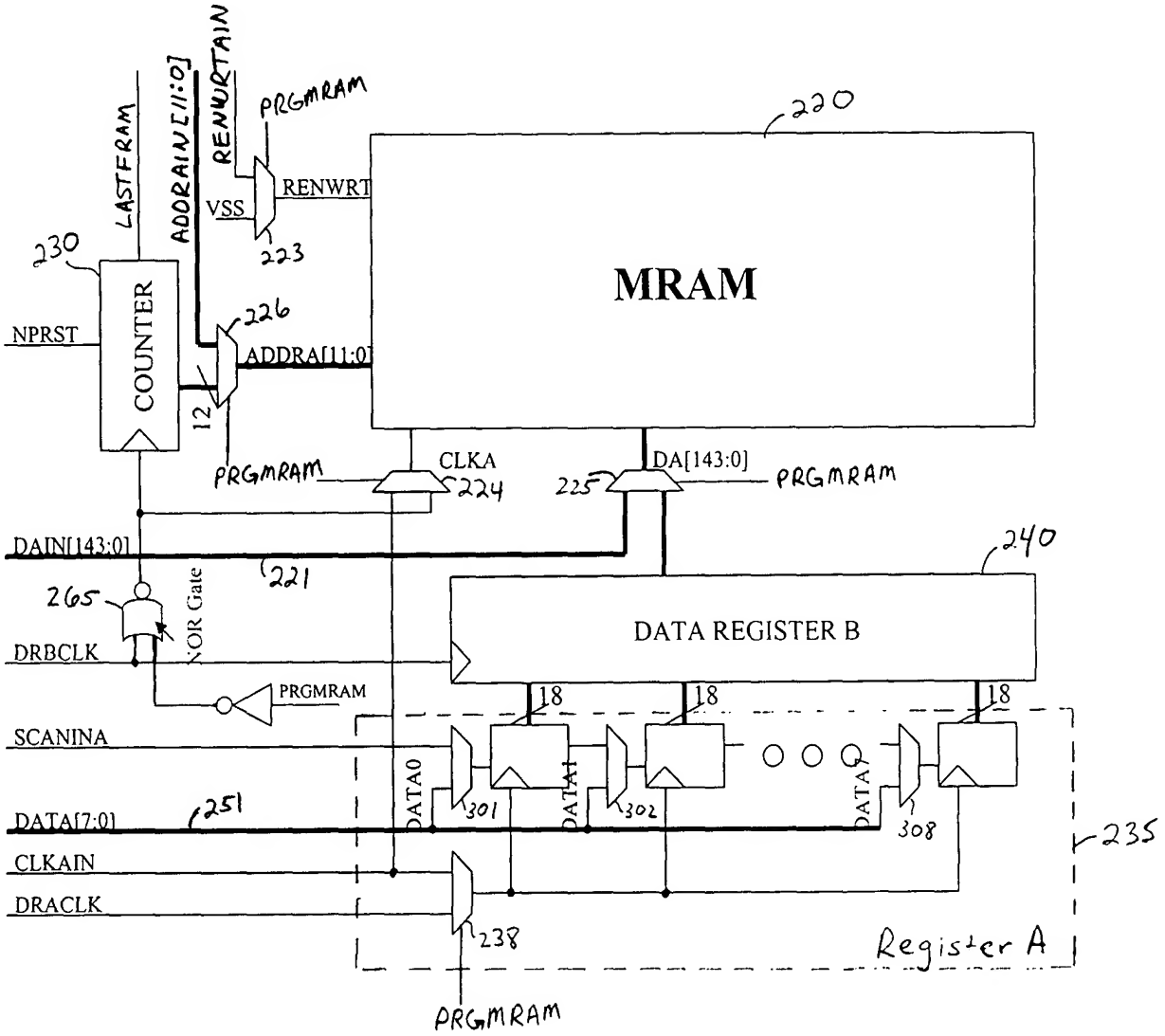
LASTFRAM
ADDRAINE[11:0]
RENWRTAIN
PRGMRAM
220
RENWRT
VSS
223
230
MRAM
COUNTER
NPRST
226
ADDRA[11:0]
12
PRGMRAM
CLKA
224
225
DA[143:0]
PRGMRAM
240
DAIN[143:0]
221
265
NOR Gate
DRBCLK
DATA REGISTER B
PRGMRAM
18
18
18
SCANINA
DATA0
DATA1
DATA7
301
302
308
235
DATA[7:0]
251
CLKAIN
DRACLK
238
Register A
PRGMRAM

FIG. 2

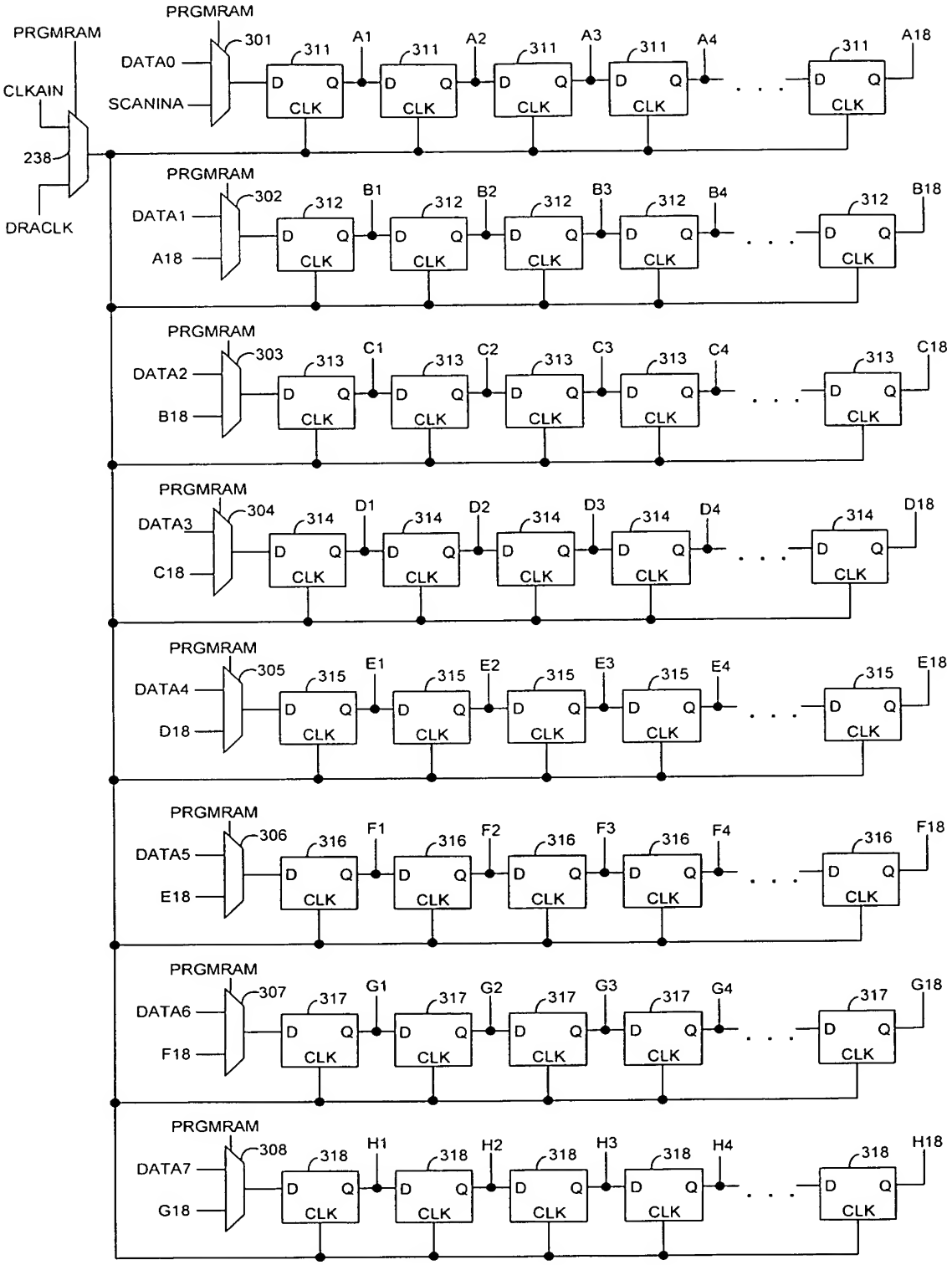
PRGMRAM
CLKAIN
238
DRACLK
PRGMRAM
301
DATA0
SCANINA
311
A1
A2
A3
A4
A18
CLK
PRGMRAM
302
DATA1
A18
312
B1
B2
B3
B4
B18
PRGMRAM
303
DATA2
B18
313
C1
C2
C3
C4
C18
PRGMRAM
304
DATA3
C18
314
D1
D2
D3
D4
D18
PRGMRAM
305
DATA4
D18
315
E1
E2
E3
E4
E18
PRGMRAM
306
DATA5
E18
316
F1
F2
F3
F4
F18
PRGMRAM
307
DATA6
F18
317
G1
G2
G3
G4
G18
PRGMRAM
308
DATA7
G18
318
H1
H2
H3
H4
H18
D
Q
CLK

FIG. 3

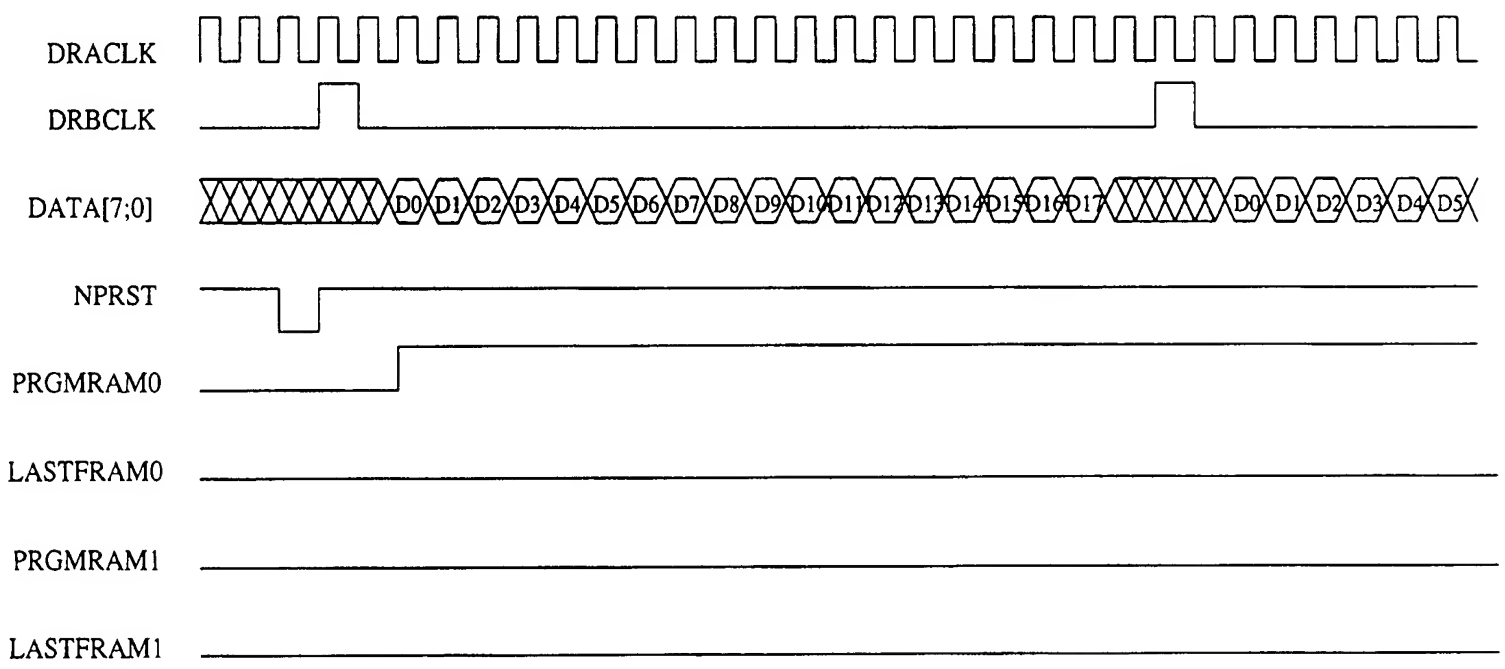

Figure 4: MRAM preload timing diagram (The beginning of MRAM0).

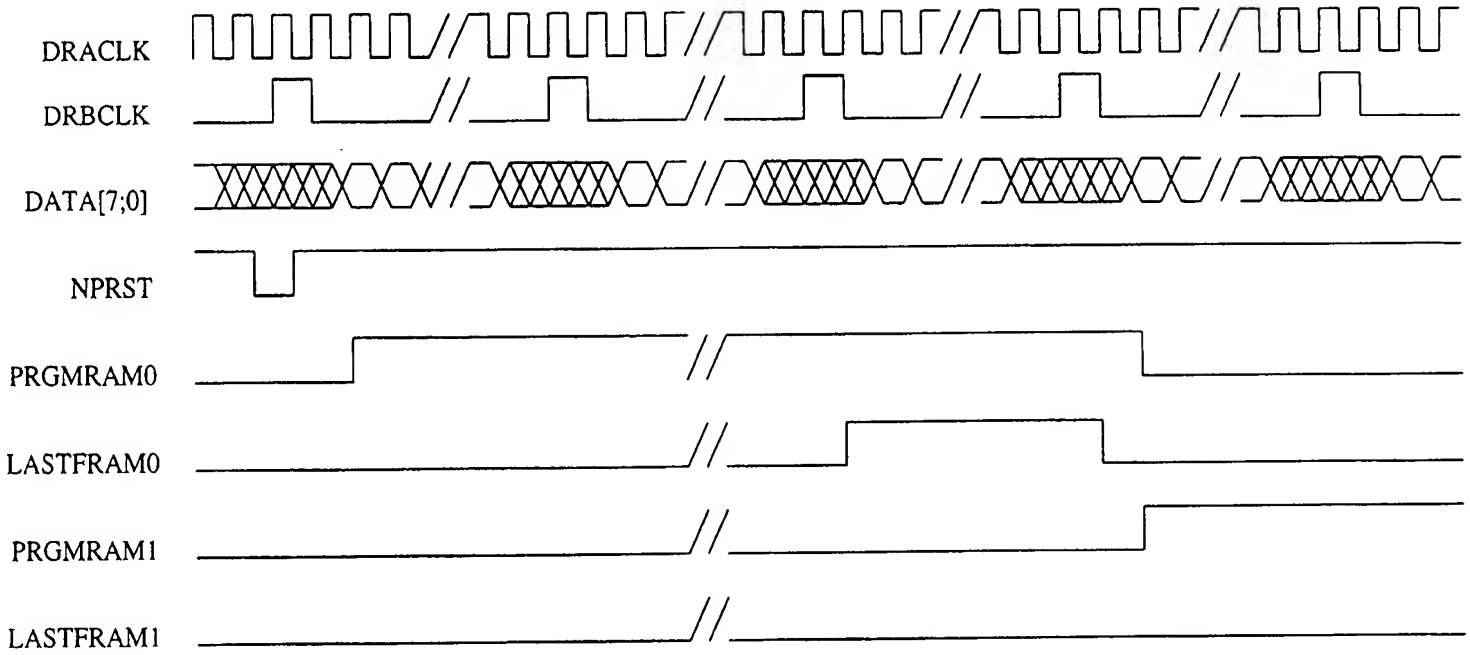

Figure 5: **Chip level MRAM preload timing diagram.**

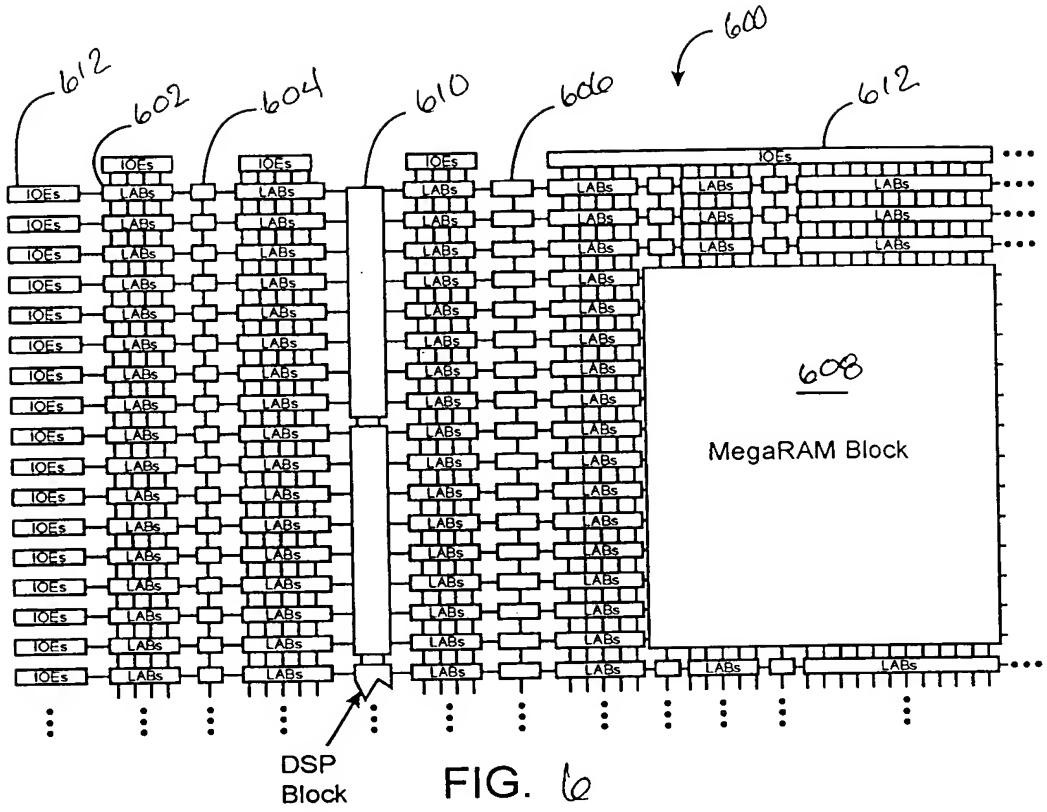
600
612
602
604
610
606
612
IOEs
LABs
608
MegaRAM Block
DSP
Block

FIG. 6

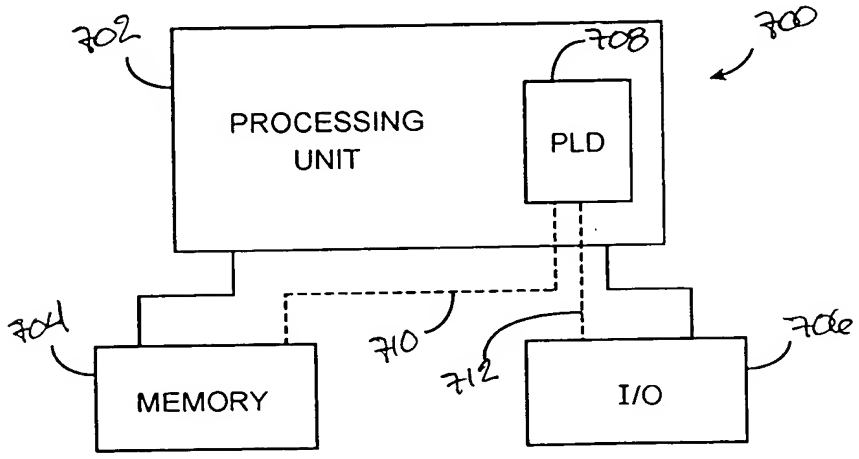
702
708
700
PROCESSING
UNIT
PLD
704
710
712
706
MEMORY
I/O

FIG. 7